UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/431,593	11/01/1999	YOSHINORI UEDA	2271/60617	8935

7590 02/11/2003

IVAN S KAVRUKOV
COOPER & DUNHAM LLP
1185 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

EXAMINER
WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/431,593	UEDA, YOSHINORI	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Applicant's Remarks filed on January 2, 2003.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 5, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Groover, III et al. (US 4,804,636).

Groover, III et al. shows (fig. 9a – 9e) a semiconductor device comprising a Si substrate and a resistance pattern (moat) formed on the substrate. The pattern comprises a first resistance pattern (poly-si) on the substrate at a first level and a second resistance pattern (source/drain or moat) provided adjacent the first resistance

pattern at a second level (in the substrate) lower than the first level. The second resistance pattern is connected in series to the first resistance pattern through a TiN local interconnect and has an edge defined by the first resistance pattern (moat is doped by a self aligning process-col. 20, lines 55-56) . The resistance pattern comprises an interlayer insulation pattern (gate oxide) under the first resistance pattern and the second resistance pattern is lower than the insulating layer. The first resistance pattern includes a polysilicon pattern and a polycide region ($TiSi_2$). The device further comprises a MOS transistor having a polysilicon gate that is identical in composition to the polysilicon pattern. The second resistance pattern is formed in the substrate in the form of a salicide region ($TiSi_2$) defined by the first resistance pattern (moat is doped by a self aligning process-col. 20, lines 55-56) .

Claims 1-3, 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Naem (US 5,911,114).

Naem discloses (fig. 1E and col. 2, line 50 – col. 3, line 12) a semiconductor device comprising a Si substrate and a resistance pattern formed on the substrate. The pattern comprises a first resistance pattern (on Field OXide region) on the substrate at a first level and a second resistance pattern (source/drain) provided adjacent the first resistance pattern at a second level (in the substrate) lower than the first level. The second resistance pattern is electrically connected in series to the first resistance pattern through a TiN local interconnect to form the resistance element and has an edge defined by the first resistance pattern (edge of FOX region) . The resistance pattern

comprises an interlayer insulation pattern (gate dielectric) under the first resistance pattern and the second resistance pattern is lower than the insulating layer. The first resistance pattern includes a polysilicon pattern and a polycide region. The device further comprises a MOS transistor having a polysilicon gate that is identical in composition to the polysilicon pattern. The second resistance pattern is formed in the substrate in the form of a salicide region defined by the first resistance pattern. The substrate includes an impurity element with a concentration level such that a parasitic MOS transistor is formed of the first resistance pattern acting as a gate electrode and a pair of second resistance patterns at both lateral sides of the first pattern and acting as source drain regions (the device is a MOS transistor col. 2, lines 50-56). Because the device is a MOS transistor, the threshold voltage is large than a supply voltage used in the device. The pattern includes a second polysilicon pattern and polycide (14) and having an impurity concentration level larger than the concentration of the first pattern due to the doping provided by the polycide process (col. 3, lines 1-7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naem (US 5,911,114).

Naem shows all of the elements of the claims except the first resistance pattern and the second resistance pattern having identical resistance. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a first and second resistance pattern having identical resistance values, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide first and second resistance patterns having identical resistance values to form a device having a desired total resistance.

Response to Arguments

Applicant's arguments filed with respect to claims 1-8 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the elements of the claims, specifically that the references of Grover or Naem do not show a first resistance pattern provided on a substrate at a first level and a second resistance pattern provided adjacent to the first pattern at a second level lower than the first level, the second resistance pattern being electrically connected in series to the first pattern to form the resistance element, the second resistance pattern having an edge defined by the first resistance pattern. The examiner maintains the previous rejection because the cited art discloses such configurations. Take for instance

Groover III in figure 9 discloses an upper resistance pattern (POLY) which is gate electrode and a lower resistance pattern (MOAT). In the broadest sense of the term resistance pattern, any material in known in the art of semiconductors provides resistance and this is a resistance pattern. When taken in this view, the gate of Groover including the sidewall oxide and gate dielectric is an upper resistance pattern and the source/drain regions including the silicide layer ($TiSi_2$) is a lower resistance pattern. It can also be seen that the edge of the upper resistance pattern defines the lower resistance pattern. The upper resistance pattern and the lower resistance pattern are connected in series by the local interconnect (TiN). The process of making the device (col. 21, lines 5-15) further disclose that an LDD implant to form part of the second resistance pattern below the first resistance pattern comes after the gate polysilicon has by deposited and etched. Then the sidewall spacers are formed on the gate (see specifically steps 7-10). Thus, the edge of the second resistance pattern is defined by the first resistance pattern. A similar configuration is seen in the figures of Naem. Therefore the cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW
MEW
February 10, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800